49	11	((leadframe and (sink or spreader or dissipating or heat) and ((cure or curing) with epoxy)) and (@ad<19990831)) and (encapsulants or encpasulate or ((outer or second) near encapsulant))	USPAT; EPO; JPO; DERWENT; IBM_TDB	2004/08/17 16:18
48	94	(leadframe and (sink or spreader or dissipating or heat) and ((cure or curing) with epoxy)) and (@ad<19990831)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/08/17 16:32
50	154	257/790.ccls. and (@ad<19990831) and (sink or spreader or heat or dissipating)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/08/17 17:31
51	26	(257/790.ccls. and (@ad<19990831) and (sink or spreader or heat or dissipating)) and ((cure or curing or cured or solidify or solid or hardened) with epoxy)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/08/17 16:34
52	31	(epoxy with underfill) and (@ad<19990831) and ((sink or spreader or heat or dissipating) with (plate or substrate)) and (encapsulant or encapsulate)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/08/17 17:33
53	46	(epoxy with (underfill or interface)) and (@ad<19990831) and ((sink or spreader or heat or dissipating) with (plate or substrate)) and (encapsulant or encapsulate)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/08/17 17:48
54	18	((epoxy with (underfill or interface)) and (@ad<19990831) and ((sink or spreader or heat or dissipating) with (plate or substrate)) and (encapsulant or encapsulate)) and (epoxy with (cure or curing))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/08/17 17:36
55	116	(epoxy with (underfill or interface)) and (@ad<19990831) and (sink or spreader or heat or dissipating) and (encapsulant or encapsulate)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/08/17 17:48
56	116	((epoxy with (underfill or interface)) and (@ad<19990831) and (sink or spreader or heat or dissipating) and (encapsulant or encapsulate)) and (@ad<19990831)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/08/17 17:49
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-	37	(((cure or harden or solidify or curing) and microwave and (sink or spreader or dissipating or thermal or heat)) with epoxy)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/08/16 21:04
-	19	((((cure or harden or solidify or curing) and microwave and (sink or spreader or dissipating or thermal or heat)) with epoxy)) and (@ad<19990831)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/08/16 21:23
-	11	(((((cure or harden or solidify or curing) and microwave and (sink or spreader or dissipating or thermal or heat)) with epoxy)) and (@ad<19990831)) and (chip or die or ic or circuit or semiconductor)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/08/16 21:09
-	14	361/701.ccls. and ((sink or spreader or heat or thermal or dissipating) with epoxy) and (chip or die or ic or circuit or semiconductor)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/08/16 21:33

-	8	361/701.ccls. and ((sink or spreader or heat or thermal or dissipating) with epoxy) and (chip or die or ic or circuit or semiconductor) and (@ad<19990831)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/08/16 21:18
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-	0	((361/702.ccls. and ((sink or spreader or heat or thermal or dissipating) with epoxy) and (chip or die or ic or circuit or semiconductor) and (@ad<19990831)) not (361/701.ccls. and ((sink or spreader or heat or thermal or dissipating) with epoxy) and (chip or die or ic or circuit or semiconductor) and (@ad<19990831))) and (((cure or curing) with epoxy) and microwave)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/08/16 21:22
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-	0	(361/703.ccls. and ((sink or spreader or heat or thermal or dissipating) with epoxy) and (chip or die or ic or circuit or semiconductor) and (@ad<19990831)) and (((cure or curing) with epoxy) and microwave)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/08/16 21:31
-	1015	(((cure or curing) with epoxy) and microwave)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/08/16 21:22
-	218	((((cure or curing) with epoxy) and microwave)) and ((sink or spreader or heat or thermal or dissipating) with epoxy) and (chip or die or ic or circuit or semiconductor)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/08/16 21:23
-	110	(((((cure or curing) with epoxy) and microwave)) and ((sink or spreader or heat or thermal or dissipating) with epoxy) and (chip or die or ic or circuit or semiconductor)) and (@ad<19990831)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/08/16 21:40
-	6	((((((cure or curing) with epoxy) and microwave)) and ((sink or spreader or heat or thermal or dissipating) with epoxy) and (chip or die or ic or circuit or semiconductor)) and (@ad<19990831)) and ((sink or spreader or (heat near dissipating) or (thermal near (dissipating or element))) with epoxy) and (chip or die or ic or circuit or semiconductor) and (@ad<19990831)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/08/16 21:26
-	129	361/704.ccls. and ((sink or spreader or heat or thermal or dissipating) with epoxy) and (chip or die or ic or circuit or semiconductor) and (@ad<19990831)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/08/16 21:31

-	0	(361/704.ccls. and ((sink or spreader or heat or thermal or dissipating) with epoxy) and (chip or die or ic or circuit or semiconductor) and (@ad<19990831)) and (((cure or curing) with epoxy) and microwave)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/08/16 21:33
-	96	257/722.ccls. and ((sink or spreader or heat or thermal or dissipating) with epoxy) and (chip or die or ic or circuit or semiconductor)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/08/16 21:34
-	0	(257/722.ccls. and ((sink or spreader or heat or thermal or dissipating) with epoxy) and (chip or die or ic or circuit or semiconductor)) and (((cure or curing) with epoxy) and microwave)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/08/16 21:34
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-	1	(257/707.ccls. and ((sink or spreader or heat or thermal or dissipating) with epoxy)) and (((cure or curing) with epoxy) and microwave)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/08/16 21:35
-	103	257/723.ccls. and ((sink or spreader or heat or thermal or dissipating) with epoxy)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/08/16 21:35
-	2	(257/723.ccls. and ((sink or spreader or heat or thermal or dissipating) with epoxy)) and (((cure or curing) with epoxy) and microwave)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/08/16 21:36
-	92	257/704.ccls. and ((sink or spreader or heat or thermal or dissipating) with epoxy)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/08/16 21:36
-	1	(257/704.ccls. and ((sink or spreader or heat or thermal or dissipating) with epoxy)) and (((cure or curing) with epoxy) and microwave)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/08/16 21:36
-	38	257/705.ccls. and ((sink or spreader or heat or thermal or dissipating) with epoxy)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/08/16 21:36
-	0	(257/705.ccls. and ((sink or spreader or heat or thermal or dissipating) with epoxy)) and (((cure or curing) with epoxy) and microwave)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/08/16 21:40
-	79	(((cure or curing) and microwave) with epoxy)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/08/16 21:40
-	44	((((cure or curing) and microwave) with epoxy)) and (@ad<19990831)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/08/17 15:08
-	1	("6764882").PN.	USPAT	2004/08/17 13:34

L Number	Hits	Search Text	DB	Time stamp
33	44	((((cure or curing) and microwave) with epoxy)) and (@ad<19990831)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/08/17 15:56
35	4	((((((cure or curing) and microwave) with epoxy)) and (@ad<19990831)) and ((cure or curing) with microwave)) and (chip or die)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/08/17 15:10
34	32	(((((cure or curing) and microwave) with epoxy)) and (@ad<19990831)) and ((cure or curing) with microwave)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/08/17 15:54
36	572	(Chip or die) and ((cure or curing) with (epoxy and (enhance or increase)))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/08/17 15:55
37	572	((Chip or die) and ((cure or curing) with (epoxy and (enhance or increase)))) and ((cure or curing) with (enhance or increase))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/08/17 15:58
38	209	((Chip or die) and ((cure or curing) with (epoxy and (enhance or increase)))) and (epoxy with adhesive)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/08/17 15:56
40	99	(((Chip or die) and ((cure or curing) with (epoxy and (enhance or increase)))) and (epoxy with adhesive)) and (@ad<19990831)	USPAT; EPO; JPO; DERWENT; IBM_TDB	2004/08/17 15:57
41	69	((((Chip or die) and ((cure or curing) with (epoxy and (enhance or increase)))) and (epoxy with adhesive)) and (@ad<19990831)) and ((cure or curing) with (bond or bonding or strength))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/08/17 16:02
42	704	((chip or die) and (lead or leads)) and (encapsulants or ((outer or second) near encapsulant))	USPAT; EPO; JPO; DERWENT; IBM_TDB	2004/08/17 16:17
43	103		USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/08/17 17:49
44	103		USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/08/17 16:34
45	96		USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/08/17 16:11
46	57	257/666.ccls. and (sink or spreader or dissipating or heat) and ((cure or curing) with epoxy)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/08/17 16:16
47	183	leadframe and (sink or spreader or dissipating or heat) and ((cure or curing) with epoxy)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/08/17 16:17

Prev cited Agen

DERWENT-ACC-NO: 1987-084066

DERWENT-WEEK: 198712

TITLE: Metallisation of ceramic for PCB of IC - by baking mixt. of copper cpd., silica, alumina with zinc or zinc cpd. at relatively low temp. and reducing

PATENT-ASSIGNEE: AGENCY OF IND SCI & TECHNOLOGY[AGEN]

PRIORITY-DATA: 1985JP-0176588 (August 9, 1985)

PATENT-FAMILY:

PUB-NO	PUB-DATE	LANGUAGE	PAGES	MAIN-IPC
JP 62036091 A	February 17, 1987		004	N/A
JP 90032235 B	July 19, 1990		000	N/A

APPLICATION-DATA:

PUB-NO	APPL-DESCRIPTOR	APPL-NO	APPL-DATE
JP 62036091A	N/A	1985JP-0176588	August 9, 1985
JP 90032235B	N/A	1985JP-0176588	August 9, 1985

INT-CL (IPC): C04B041/88

ABSTRACTED-PUB-NO: JP 62036091A

BASIC-ABSTRACT:

A mixt. consisting of at least one of CuCO3, CuSO4, CuS, CuO and CuCl2, at least one of SiO2 and kaolin, and at least one of Zn and Zn cpds. is coated on the surface of the ceramic, baking at 900-1300 deg.C in oxidising atmos., then reducing the baked layer.

seal 202, an interface with a low thermal resistance is created between the die 211 and the protrusion 201 on the heat spreader 200. Since thermal resistance in the interface is reduced, heat generated by the die 211 is better transferred to the heat spreader 200 for dissipation. The improved heat transfer process improves the life expectancy of the package and reduces the chance that semiconductor device 211 will fail.

Detailed Description Text - DETX (7):

Referring now to FIG. 3, another embodiment of the invention is shown which includes a heat spreader 300 having a protrusion 301 formed on its bottom surface. Having the protrusion 301 on the heat spreader 300 results in the heat spreader effectively being placed closer to the semiconductor die 311. As discussed above, the closer heat spreader 300 can be placed to the semiconductor die 311, the less thermal resistance is created by the interface between them, and heat transfer processes flowing from the die to the heat spreader are improved. However, due to the different thermal expansion coefficients of the semiconductor device and the heat spreader material, the metal-to-metal seal of the above embodiment may in some cases be lost during heating. Thus, the present invention also provides for an interface 302 between the protrusion 301 and the semiconductor die 311 which comprises a thin layer of epoxy, e.g., for example, such as "LOCTITE-384", available from Loctite Corp., for providing and maintaining permanent contact between the protrusion 301 and the semiconductor die 311 during heating and cooling of the device. Alternatively, a thermally conductive tape, for example, such as "T-Flex" 440, available from Thermagon, Inc., may be substituted in place of the thin layer of epoxy. While the thermal conductivity of both epoxy and tape is relatively low and therefore creates an additional undesirable thermal resistance in the interface 302, the additional resistance is still much lower than with conventional heat spreaders 300 because the layer of epoxy or tape is very thin due to the extension of the protrusion 301 toward the non-active surface of the semiconductor die 311. Put another way, with conventional heat spreaders, the layer of interface material is very thick because there is no protrusion extending from the bottom surface of the heat spreader toward the back surface of the die and thus the thermal resistance in the heat transfer

Metal

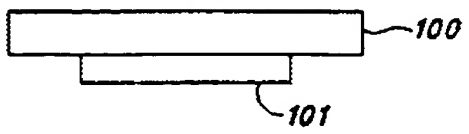

FIG. 1B

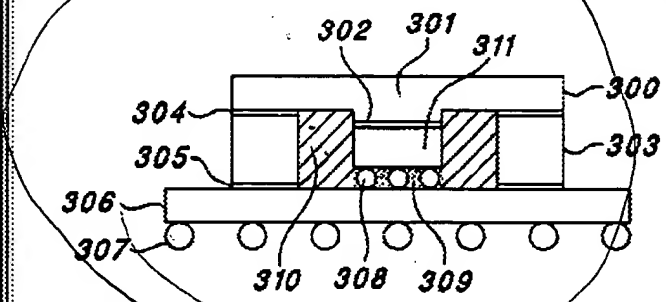

FIG. 3

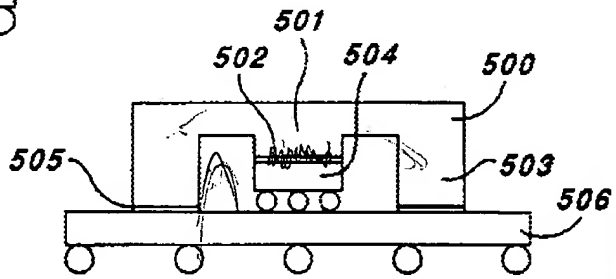

FIG. 5

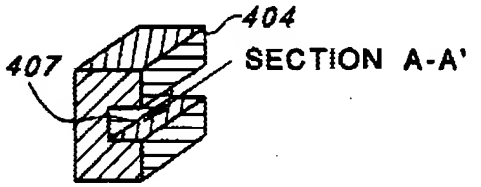

FIG. 4B

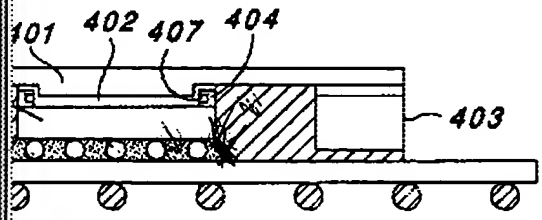

FIG. 4C

FIG. 2b by the use of an electrically nonconductive adhesive such as epoxy. The aluminum plate stiffens the resulting composite printed circuit board, and allows components to be mounted from the "component" side, whereby the "circuit" side (which as mentioned is the underside illustrated in FIGS. 1 and 2), may be passed through a standard wave soldering apparatus for low cost assembly. If desired, the components, such as component 26 illustrated in FIG. 1, may be clamped to the upper surface of aluminum plate 24 to enhance heat transfer away from the component toward a thermal sink (not illustrated). FIG. 3 illustrates a cross section through a component mounted on a composite printed circuit board such as that described in conjunction with FIGS. 1 and 2. In FIG. 3, elements corresponding to those of FIGS. 1 and 2 are designated by the same reference numerals. In FIG. 3, component 26 is illustrated in outline as a transistor, a mounting plate 49 of which is clamped against the upper surface of conductive plate 24 by a screw 50, which passes through mounting hole 32 and screws into a mounting post 52. Mounting post 52 bears against the lower side of ground plating 18. As also illustrated in FIG. 3, conductive plate 24 is mounted to the upper surface of ground plane 14 by means of a nonconductive epoxy 54. The thickness of epoxy 54 may vary, so that the lower surface of conductive plate 24 may make electrical contact with the upper surface of ground plane 14 at various points, such as point 56. Also, if any burrs remain from the drilling of holes 34 or 36, or 40 or 42, the burrs may penetrate through epoxy 54 to make contact. Even if epoxy 54 is rendered conductive by the addition of a solid conductive filler such as silver particles, the contact such as at point 56 will tend to change the impedance of the ground paths. Such uncontrolled ground plane connections may be disadvantageous as described in the aforementioned Meier article, and should be avoided in any manufacturing process making production quantities as opposed to one-of-a-kind items.

United States Patent [19]
Iannacone et al.

[11] Patent Number: 4,975,142
[45] Date of Patent: Dec. 4, 1990

[54] **FABRICATION METHOD FOR PRINTED CIRCUIT BOARD**

[75] Inventors: Joseph M. Iannacone, Bensalem, Pa.; Lawrence J. Ibbetson, Mount Laurel, N.J.

[73] Assignee: General Electric Company, Moorestown, N.J.

[21] Appl. No.: 433,066

[22] Filed: Nov. 7, 1989

[51] Int. Cl.[5] B44C 1/22; C23F 1/02; C03C 15/00; B29C 37/00

[52] U.S. Cl. 156/630; 29/852; 156/634; 156/644; 156/645; 156/655; 156/659.1; 156/902; 427/97

[58] Field of Search 156/630, 634, 644, 645, 156/656, 659.1, 661.1, 666, 668, 901, 902; 29/846, 852; 174/68.5; 427/96, 97; 430/313, 317, 318; 361/395, 397, 400, 401, 403, 413; 204/15

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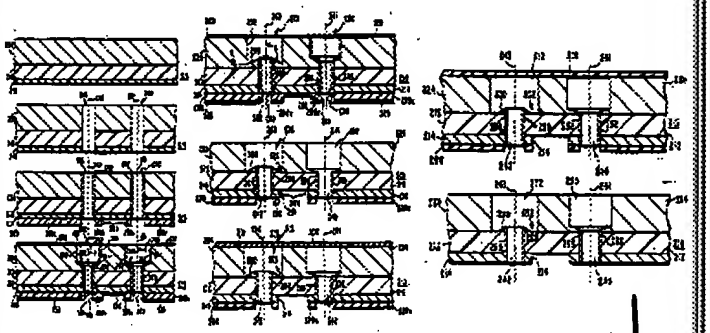
"Miniaturized Microwave Packaging—A Different Game" by Markstein, published in the Aug., 1982 issue of Electronic Packaging and Production.
"Printed Circuit Integration of MW Filters" by Rooney et al., published at pp. 2-6 of the Microwave Journal and distributed by Rogers Corporation.
"Microwave Stripline Packaging with VMDS" by Trent, published in Microwave Journal, Aug. 1975.

Primary Examiner—William A. Powell
Attorney, Agent, or Firm—William H. Meise

[57] **ABSTRACT**

A double-sided printed circuit board includes a component side and a circuit side. The dielectric material is undesirably flexible. To render the board rigid, the conductor bonded to the component side is a rigid plate. At locations at which plated-through component signal leads are to be attached, lead clearance holes are drilled through all the way through the thin conductor, the dielectric, and the plate. The holes are plated with conductor. From the exposed side of the plate, larger holes are drilled coaxial with the clearance holes, part-way through the plate. The hole bottoms make an acute angle with the axes. The exposed surfaces are plated with etch resist. A second depth-controlled drilling coaxial with the first is performed with a drill which has a reverse-angle face, to a depth which extends almost through the plate, to thereby remove etch resist in an annular region surrounding the original clearance hole. The plate is etched sufficiently to free an annular region around each clearance hole from conductor.

6 Claims, 8 Drawing Sheets



L13, L22-24

include a more complex profile such as achieved with an etching process. Through holes **120**, **122** and **124** have diameters of 50 microns or larger, preferably larger than 100 microns, to simply fabrication.

As is described in greater detail hereinbelow, representative through holes **120** and **122**, and device main terminal **108** on active major surface **104**, are in alignment. Device main terminal **108** may be a source terminal **108**, and serves as a high current terminal. The number and size of through holes **120** and **122** depend upon device **102** size, contact pad **108** size and shape, and the current requirements of device **102**. Typically, for a device **102** carrying from 10 to 500 amps of ON current, 10 to 100 through holes **120** and **122** with diameters in the range of 100 to 500 microns could be employed. Fewer through holes **120** and **122** could be employed with larger openings, such as from 1 to 10 through holes, with diameters within the range of 500 to 5,000 microns. Thus, in an extreme case a single large through hole **120** or **122** may be provided for alignment with representative drain source contact **108**. Multiple connections formed with through holes **120** and **122** to a single contact pad provide a connection which is superior to a single wire bond.

Active major surface **104** of device **102** is bonded to second side **118** of the sheet of dielectric film **114**, with contact pads **108** and **110** and corresponding ones of through holes **120**, **122** and **124** in alignment as described above.

More particularly, with reference to FIG. **2**, an adhesive layer **126** is deposited on to second side **118** of dielectric film **114**, which second side **118** is on the underside of film **114** in the orientation of FIG. **2**, but would be oriented as the top side during a typical fabrication process. Adhesive layer **126** can be either a thermoset or a thermoplastic polymeric material, preferably a low temperature cure thermoset to minimize high temperature processing. A suitable material for adhesive layer **126**, for example is an ULTRADEL™ adhesion promoter (ULTRADEL is a trademark of Amoco Chemicals) with a thickness within the approximate range of 10 to 20 microns.

FIG. **3** shows power semiconductor device **102**, still un-packaged, mounted active major surface **104** down (since the orientation of FIG. **3** is inverted) onto adhesive layer **126** on second side **118** of dielectric film **114**. Device **102** contact pads **108** and **110** are aligned to preformed through holes **120**, **122** and **124** in film **114**. Device **102** may be bonded in place using a thermal curing cycle and, if required, a vacuum to facilitate removal of entrapped air and outgassing from adhesive **126**. Alternative curing options include a microwave cure and an ultraviolet light cure, for example.

With reference to FIG. **4**, which likewise is inverted in orientation, a dielectric encapsulant **130** is molded around semiconductor device **102** on second side **118** of dielectric film **114**. Molding material to form dielectric encapsulant **130** is poured or injected into a mold form (not shown) in a manner optimizing environmental conditions such as temperature, atmosphere, and pressure, to minimize voids, stresses, shrinkage and other potential defects. Typically, the process step of molding dielectric encapsulant **130** is preformed in a vacuum, preferably at a processing temperature that does not exceed 300° C.

Dielectric encapsulant **130** may comprise a plastic encapsulant such as an epoxy with a high level of inorganic particle fill (such as 70% silica) that is molded around device **102** and thermally cured (or cured with another process such as UV light cure or microwave cure) to form a protective structure for the resultant device package **100**. Particularly in

Details | Text | Image | HTML | Full

Prev cited

USO06306680B1

(12) **United States Patent**
Fillion et al.

(10) **Patent No.:** **US 6,306,680 B1**
(45) **Date of Patent:** **Oct. 23, 2001**

(54) POWER OVERLAY CHIP SCALE PACKAGES FOR DISCRETE POWER DEVICES

(75) Inventors: Raymond Albert Fillion, Schenectady; Barry Scott Whitmore, Waterford; Charles Steven Korman, Schenectady, all of NY (US); Albert Andrew Maria Esser, Delafield, WI (US)

(73) Assignee: General Electric Company, Schenectady, NY (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: 09/258,412

(22) Filed: Feb. 22, 1999

(51) Int. Cl.⁷ H01L 21/44; H01L 21/48; H01L 21/50; H01L 21/30

(52) U.S. Cl. 438/106; 438/107; 438/108; 428/109; 438/456; 438/517

(58) Field of Search 438/107, 109, 438/110, 112, 121, 456, 612, 617, 106, 108, 124, 125, 126, 113

(56) **References Cited**

U.S. PATENT DOCUMENTS

[illegible]

* cited by examiner

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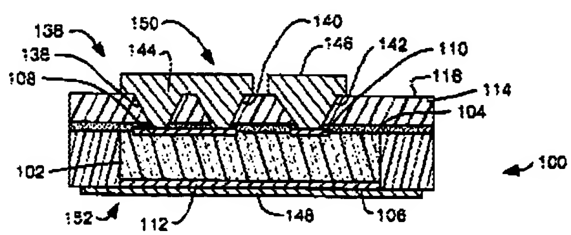
Assistant Examiner—Chuong Luu

(57) **ABSTRACT**

A power semiconductor device package includes at least one power semiconductor device mounted onto at least one electrically and thermally conductive spacer having an upper end surface bonded to a back surface of the device; a substrate of hardened substrate molding material surrounding the semiconductor device and the spacer except for an active major surface of the device and an lower end surface of the spacer; a dielectric film overlying the device active major surface and a top side of the substrate, the dielectric layer having a plurality of holes aligned with predetermined ones of the contact pads; a top side patterned metal layer on the dielectric film including portions extending into the holes electrically and thermally connected to contact pads of the device; and a backside metal layer on a substrate bottom side electrically and thermally connected to the spacer lower end surface. Optional through-post structures can be employed to bring all electrical connections either to the top side of the device package or the bottom side. Optional heat sinks can be mounted to the top side, the bottom side, or both sides.

26 Claims, 22 Drawing Sheets



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engagement through the plastic encapsulation process.

(7) After the heat sink 50 and the die-attach paddle 58 are compression fitted together, as shown in FIGS. 6a and 6b, an integrated circuit die 66 is bonded to the top surface 54 of the heat sink 50 in a recessed area 74 surrounded by the raised ridge 52 by an adhesive layer 78. The adhesive layer 78 has high thermal conductivity and can be cured in a short time to a maximum bond strength. The adhesive may be a polymeric based adhesive such as an epoxy, loaded with a metal filler of silver powder. The epoxy adhesive provides a short cure time and a high bond strength while silver powder improves its thermal conductivity such that heat generated in the integrated circuit die 66 can be rapidly conducted to the heat sink 50. The die bonding operation can be carried out in a pair of mold platens (not shown) by applying a pressure thereon to form a tight bond between the die 66 and the heat sink 50.

(8) After the die bonding process, bonding wires 82 are provided between the bonding pads 68 situated on the top surface 70 of IC die 66 and the leads (not shown) on lead frame 58. This enables the connection of the IC die 66 to the outside circuit that the plastic molded package 90 is connected to. The number of bonding pads 68 situated on the top surface 70 of die 66 can be numerous and is dependent on the size of the IC die 66. After the completion of the wire bonding process, the assembly of the IC die 66, the heat sink 50, and the die-attach paddle 58 in lead frame 56 are placed in an injection mold apparatus (not shown) and a plastic material 84 is subsequently injected to completely encapsulate and to form a plastic molded package 90. The plastic encapsulation protects the various components from damages by mechanical force, by moisture, by heat and by chemicals.

(9) In a first alternate embodiment, a heat sink 94 that has a raised top 96 instead of a raised ridge 52 (shown in FIG. 6b) is used. This is shown in FIG. 8. The heat sink 94 frictionally engages the die-attach paddle 98 at the

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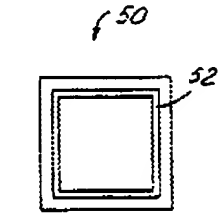

FIG. 4A

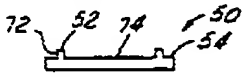

FIG. 4B

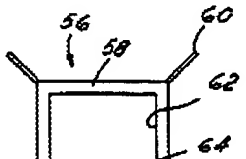

FIG. 5

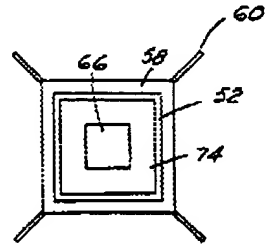

FIG. 6A

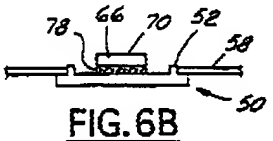

FIG. 6B

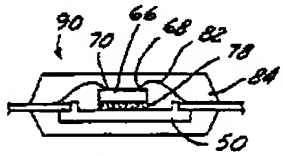

FIG. 7

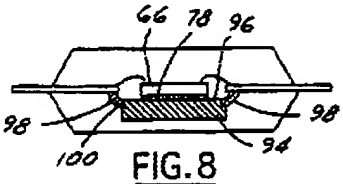

FIG. 8

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Detailed Description Text - DETX (7):

After the heat sink 50 and the die-attach paddle 58 are compression fitted together, as shown in FIGS. 6a and 6b, an integrated circuit die 66 is bonded to the top surface 54 of the heat sink 50 in a recessed area 74 surrounded by the raised ridge 52 by an adhesive layer 78. The adhesive layer 78 has high thermal conductivity and can be cured in a short time to a maximum bond strength. The adhesive may be a polymeric based adhesive such as an epoxy, loaded with a metal filler of silver powder. The epoxy adhesive provides a short cure time and a high bond strength while silver powder improves its thermal conductivity such that heat generated in the integrated circuit die 66 can be rapidly conducted to the heat sink 50. The die bonding operation can be carried out in a pair of mold platens (not shown) by applying a pressure thereon to form a tight bond between the die 66 and the heat sink 50.

Detailed Description Text - DETX (10):

In a second alternate embodiment of the present invention (not shown), a multiple number of integrated circuit dies are bonded and encapsulated. In applications where more than one IC die is bonded to a heat sink, the substrate is first bonded to the heat sink by an adhesive layer. The adhesive can be a similar type of adhesive that is used in bonding the IC dies to the heat sink. This technique enables the bonding of two or more integrated circuit dies to a single substrate after the substrate is bonded to a heat sink. Bonding wires are then connected between the IC dies and the substrate through electrical circuits. The substrate is then connected by connecting wires to various leads on the lead frame. The method provides greater flexibility to the present invention such that it can be applied in multiple IC package applications.

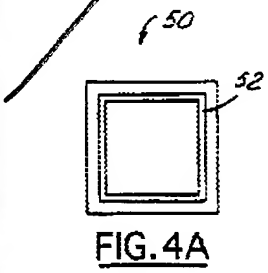

FIG. 4A

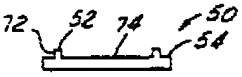

FIG. 4B

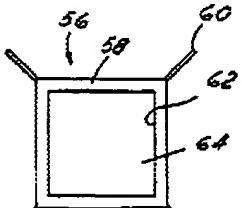

FIG. 5

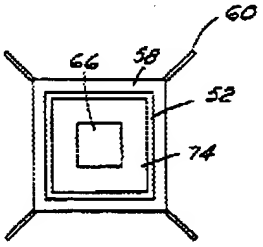

FIG. 6A

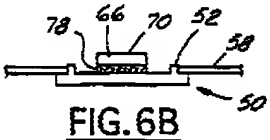

FIG. 6B

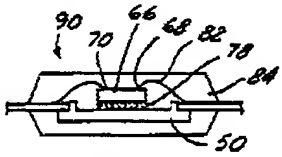

FIG. 7

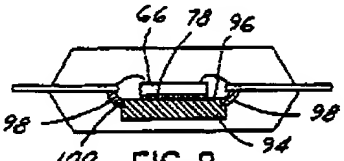

FIG. 8